1. A method for integrating low-K materials in semiconductor fabrication, comprising the steps of:

a. providing a semiconductor structure having a dielectric layer thereover; said dielectric layer being comprised of a low-K material;

b. patterning said dielectric layer to form pillar openings;

c. depositing a pillar layer over said semiconductor structure; thereby filling said pillar openings with said pillar layer; and

d. planarizing said pillar layer to form pillars embedded in said dielectric layer.

2. The method of claim 1 wherein said pillar layer comprises a material selected from the group composed of: silicon nitride, silicon carbide, amorphous carbon, carbon, tungsten, copper and aluminum.

3. The method of claim 1 wherein said pillars are formed prior to forming a dual damascene contact structure.

4. The method of claim 1 wherein said pillars are formed simultaneously with interlayer contacts.

5. A method for integrating low-K materials in semiconductor fabrication, comprising the steps of:

a. providing a semiconductor structure having a dielectric layer thereover; said dielectric layer comprising an organic low-K material;

b. patterning said dielectric layer to form pillar openings;

c. depositing a pillar layer over said semiconductor structure; thereby filling said pillar openings with said pillar layer;

d. planarizing said pillar layer to form pillars embedded in said dielectric layer;

e. patterning said dielectric layer to form via openings and trench openings;

f. forming an interconnect layer over said semiconductor structure; and

g. planarazing said interconnect layer, stopping on said dielectric layer.

6. The method of claim 5 wherein said dielectric layer comprises a material selected from the group composed of: aerogel, xerogel, nanoglass, Flare, and amorphous CF_X.

7. The method of claim 5 wherein said pillar layer comprises a material selected from the group composed of: silicon nitride, silicon carbide, amorphous carbon, carbon, tungsten, copper and aluminum.

8. The method of claim 6 wherein said pillar layer comprises a material selected from the group composed of: silicon nitride, silicon carbide, amorphous carbon, carbon, tungsten, copper and aluminum.

9. The method of claim 5 wherein a barrier layer is formed over said semiconductor structure prior to forming said interconnect layer.

10. A method for integrating low-K materials in semiconductor fabrication, comprising the steps of:

a. providing a semiconductor structure having a conductive structure thereon; said

semiconductor structure and said conductive structure having a dielectric layer thereover; said dielectric layer being comprised of a low-K material;

b. patterning said dielectric layer to form pillar openings and via openings; said via openings being over said conductive structures and said pillar openings forming a matrix pattern surrounding said conductive structures;

c. depositing a pillar and contact layer over said semiconductor structure; thereby filling said pillar openings and said via openings with said pillar and contact layer;

d. planarizing said pillar and contact layer to form pillars and contacts embedded in said dielectric layer; and

e. forming an interconnect pattern over said contacts.

11. The method of claim 10 wherein said dielectric layer is comprised of a material selected from the group composed of: aerogel, xerogel, nanoglass, Flare, and amorphous CF_X.

12. The method of claim 10 wherein said pillar and contact layer is comprised of a

material selected from the group composed of: tungsten, copper and aluminum.

13. The method of claim 11 wherein said pillar layer is comprised of a material selected from the group composed of: tungsten, copper and aluminum.